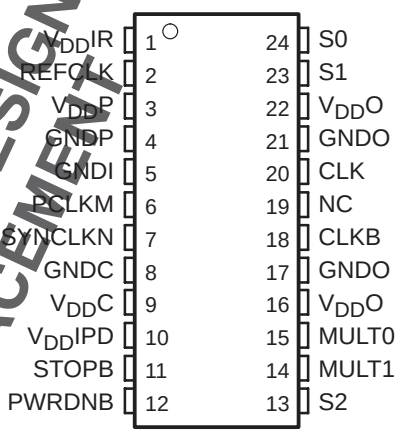
- **400-MHz Differential Clock Source for Direct Rambus™ Memory Systems for an 800-MHz Data Transfer Rate**
- **Synchronizes the Clock Domains of the Rambus Channel With an External System or Processor Clock**
- **Three Power Operating Modes to Minimize Power for Mobile and Other Power-Sensitive Applications**
- **Operates From a Single 3.3-V Supply and 120 mW at 300 MHz (Typ)**
- **Packaged in a Shrink Small-Outline Package (DBQ)**
- **Supports Frequency Multipliers: 4, 6, 8, 16/3**
- **No External Components Required for PLL**
- **Supports Independent Channel Clocking**
- **Spread Spectrum Clocking Tracking Capability to Reduce EMI**
- **Designed for Use With TI's 133-MHz Clock Synthesizers CDC924 and CDC921**
- **Cycle-Cycle Jitter Is Less Than 50 ps at 400 MHz**
- **Certified by Gigatest Labs to Exceed the Rambus DRCG Validation Requirement**
- **Supports Industrial Temperature Range of −40°C to 85°C**

DBQ PACKAGE
(TOP VIEW)



NC − No internal connection

description

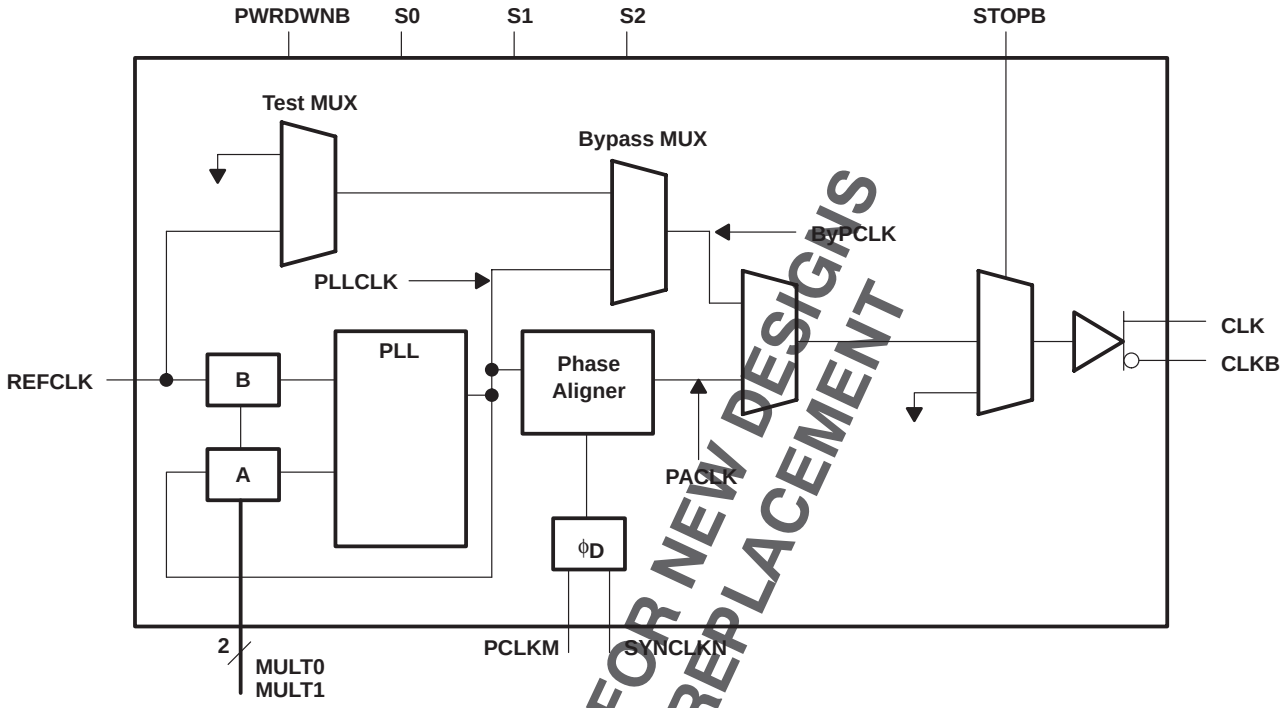
The Direct Rambus clock generator (DRCG) provides the necessary clock signals to support a Direct Rambus memory subsystem. It includes signals to synchronize the Direct Rambus channel clock to an external system or processor clock. It is designed to support Direct Rambus memory on a desktop, workstation, server, and mobile PC motherboards. DRCG also provides an off-the-shelf solution for a broad range of Direct Rambus memory applications.

The DRCG provides clock multiplication and phase alignment for a Direct Rambus memory subsystem to enable synchronous communication between the Rambus channel and ASIC clock domains. In a Direct Rambus memory subsystem, a system clock source provides the REFCLK and PCLK clock references to the DRCG and memory controller, respectively. The DRCG multiplies REFCLK and drives a high-speed BUSCLK to RDRAMs and the memory controller. Gear ratio logic in the memory controller divides the PCLK and BUSCLK frequencies by ratios M and N such that PCLKM = SYNCLKN, where SYNCLK = BUSCLK/4. The DRCG detects the phase difference between PCLKM and SYNCLKN and adjusts the phase of BUSCLK such that the skew between PCLKM and SYNCLKN is minimized. This allows data to be transferred across the SYNCLK/PCLK boundary without incurring additional latency.

User control is provided by multiply and mode selection terminals. The multiply terminals provide selection of one of four clock frequency multiply ratios, generating BUSCLK frequencies ranging from 267 MHz to 400 MHz with clock references ranging from 33 MHz to 100 MHz. The mode select terminals can be used to select a bypass mode where the frequency multiplied reference clock is directly output to the Rambus channel for systems where synchronization between the Rambus clock and a system clock is not required. Test modes are provided to bypass the PLL and output REFCLK on the Rambus channel and to place the outputs in a high-impedance state for board testing.

The CDCR83 is characterized for operation over free-air temperatures of −40°C to 85°C.

functional block diagram



FUNCTION TABLE†

MODE	S0	S1	S2	CLK	CLKB
Normal	0	0	0	Phase aligned clock	Phase aligned clock B
Bypass	1	0	0	PLLCLK	PLLCLKB
Test	1	1	0	REFCLK	REFCLKB
Output test (OE)	0	1	X	Hi-Z	Hi-Z
Reserved	0	0	1	—	—
Reserved	1	0	1	—	—
Reserved	1	1	1	Hi-Z	Hi-Z

† X = don't care, Hi-Z = high impedance

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLK	20	O	Output clock
CLKB	18	O	Output clock (complement)
GNDC	8		GND for phase aligner
GNDI	5		GND for control inputs
GNDO	17, 21		GND for clock outputs
GNDP	4		GND for PLL
MULT0	15	I	PLL multiplier select
MULT1	14	I	PLL multiplier select
NC	19		Not used
PCLKM	6	I	Phase detector input
PWRDNB	12	I	Active low power down
REFCLK	2	I	Reference clock
S0	24	I	Mode control
S1	23	I	Mode control
S2	13	I	Mode control
STOPB	11	I	Active low output disable
SYNCLKN	7	I	Phase detector input
$V_{DD}C$	9		V_{DD} for phase aligner
$V_{DD}IPD$	10		Reference voltage for phase detector inputs and STOPB
$V_{DD}IR$	1		Reference voltage for REFCLK
$V_{DD}O$	16, 22		V_{DD} for clock outputs
$V_{DD}P$	3		V_{DD} for PLL

PLL divider selection

Table 1 lists the supported REFCLK and BUSCLK frequencies. Other REFCLK frequencies are permitted, provided that (267 MHz < BUSCLK < 400 MHz) and (33 MHz < REFCLK < 100 MHz).

Table 1. REFCLK and BUSCLK Frequencies

MULT0	MULT1	REFCLK (MHz)	MULTIPLY RATIO	BUSCLK (MHz)
0	0	67	4	267
0	1	50	6	300
0	1	67	6	400
1	1	33	8	267
1	1	50	8	400
1	0	67	16/3	356

Table 2. Clock Output Driver States

STATE	PWRDNB	STOPB	CLK	CLKB
Powerdown	0	X	GND	GND
CLK stop	1	0	$V_{X,\ STOP}$	$V_{X,\ STOP}$
Normal	1	1	PACLK/PLLCLK/ REFCLK†	PACLKB/PLLCLKB/ REFCLKB

† Depending on the state of S0, S1, and S2

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) . . . . . −0.5 V to 4 V
Output voltage range, V_O, at any output terminal . . . . . −0.5 V to V_{DD} + 0.5 V
Input voltage range, V_I, at any input terminal . . . . . −0.5 V to V_{DD} + 0.5 V
Continuous total power dissipation . . . . . see Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$‡	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DBQ	1400 mW	11 mW/°C	905 mW	740 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3.135	3.3	3.465	V
High-level input voltage, V_{IH} (CMOS)	$0.7 \times V_{DD}$			V
Low-level input voltage, V_{IL} (CMOS)			$0.3 \times V_{DD}$	V
Initial phase error at phase detector inputs (required range for phase aligner)	$-0.5 \times t_{c(PD)}$		$0.5 \times t_{c(PD)}$	
REFCLK low-level input voltage, V_{IL}			$0.3 \times V_{DD}$IR	V
REFCLK high-level input voltage, V_{IH}	$0.7 \times V_{DD}$IR			V
Input signal low voltage, V_{IL} (STOPB)			$0.3 \times V_{DD}$IPD	V
Input signal high voltage, V_{IH} (STOPB)	$0.7 \times V_{DD}$IPD			V
Input reference voltage for (REFCLK) (V_{DD}IR)	1.235		3.465	V
Input reference voltage for (PCLKM and SYSCLKN) (V_{DD}IPD)	1.235		3.465	V
High-level output current, I_{OH}			−16	mA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	−40		85	°C

timing requirements

	MIN	MAX	UNIT
Input cycle time, $t_{c(in)}$	10	40	ns
Input cycle-to-cycle jitter		250	ps
Input duty cycle over 10,000 cycles	40%	60%	
Input frequency modulation, f_{mod}	30	33	kHz
Modulation index, nonlinear maximum 0.5%		0.6%	
Phase detector input cycle time (PCLKM and SYNCLKN)	30	100	ns
Input slew rate, SR	1	4	V/ns
Input duty cycle (PCLKM and SYNCLKN)	25%	75%	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{O(STOP)}$	Output voltage during CLK Stop (STOPB = 0)		See Figure 1		1.1		2	
$V_{O(X)}$	Output crossing-point voltage		See Figure 1 and Figure 6		1.3		1.8	V
V_O	Output voltage swing		See Figure 1		0.4		0.6	V
V_{IK}	Input clamp voltage		V_{DD} = 3.135 V,	I_I = −18 mA			−1.2	V
V_{OH}	High-level output voltage		See Figure 1				2	V
			V_{DD} = min to max,	I_{OH} = −1 mA	V_{DD} − 0.1 V			
			V_{DD} = 3.135 V,	I_{OH} = −16 mA	2.4			
V_{OL}	Low-level output voltage		See Figure 1		1			V
			V_{DD} = min to max,	I_{OL} = 1 mA			0.1	
			V_{DD} = 3.135 V,	I_{OL} = 16 mA			0.5	
I_{OH}	High-level output current		V_{DD} = 3.135 V,	V_O = 1 V	−32	−52		mA
			V_{DD} = 3.3 V,	V_O = 1.65 V		−51		
			V_{DD} = 3.465 V,	V_O = 3.135 V		−14.5	−21	
I_{OL}	Low-level output current		V_{DD} = 3.135 V,	V_O = 1.95 V	43	61.5		mA
			V_{DD} = 3.3 V,	V_O = 1.65 V		65		
			V_{DD} = 3.465 V,	V_O = 0.4 V		25.5	36	
I_{OZ}	High-impedance-state output current		S0 = 0, S1 = 1				±10	µA
$I_{OZ(STOP)}$	High-impedance-state output current during CLK stop		Stop = 0, V_O = GND or V_{DD}				±100	µA
$I_{OZ(PD)}$	High-impedance-state output current in power-down state		PWRDNB = 0, V_O = GND or V_{DD}		−10		100	µA
I_{IH}	High-level input current	REFCLK, PCLKM, SYNCLKN, STOPB	V_{DD} = 3.465 V,	V_I = V_{DD}			10	µA
		PWRDNB, S0, S1, S2, MULT0, MULT1	V_{DD} = 3.465 V,	V_I = V_{DD}			10	
I_{IL}	Low-level input current	REFCLK, PCLKM, SYNCLKN, STOPB	V_{DD} = 3.465 V,	V_I = 0			−10	µA
		PWRDNB, S0, S1, S2, MULT0, MULT1	V_{DD} = 3.465 V,	V_I = 0			−10	
Z_O	Output impedance	High state	R_I at I_O −14.5 mA to −16.5 mA		15	35	50	Ω
		Low state	R_I at I_O 14.5 mA to 16.5 mA		11	17	35	
	Reference current	$V_{DD}IR$, $V_{DD}IPD$	V_{DD} = 3.465 V	PWRDNB = 0			50	µA
				PWRDNB = 1			0.5	mA
C_I	Input capacitance		V_I = V_{DD} or GND			2		pF
C_O	Output capacitance		V_O = V_{DD} or GND			3		pF
$I_{DD(PD)}$	Supply current in power-down state		REFCLK = 0 MHz to 100 MHz, PWDNB = 0, STOPB = 1				100	µA
$I_{DD(CLKSTOP)}$	Supply current in CLK stop state		BUSCLK configured for 400 MHz				30	mA
$I_{DD(NORMAL)}$	Supply current in normal state		BUSCLK = 400 MHz				70	mA

† V_{DD} refers to any of the following; V_{DD}, $V_{DD}IPD$, $V_{DD}IR$, $V_{DD}O$, $V_{DD}C$, and $V_{DD}P$
‡ All typical values are at V_{DD} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER				TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{c(out)}$	Clock output cycle time				2.5		3.75	ns
$t_{(jitter)}$	Total cycle jitter over 1, 2, 3, 4, 5, or 6 clock cycles	Infinite and stopped phase alignment	267 MHz	See Figure 3			80	ps
			300 MHz				70	
			356 MHz				60	
			400 MHz				50	
$t_{(phase)}$	Phase detector phase error for distributed loop			Static phase error‡	−100		100	ps
$t_{(phase, SSC)}$	PLL output phase error when tracking SSC			Dynamic phase error‡	−100		100	ps
$t_{(DC)}$	Output duty cycle over 10,000 cycles			See Figure 4	45%		55%	
$t_{(DC, err)}$	Output cycle-to-cycle duty cycle error	Infinite and stopped phase alignment	267 MHz	See Figure 5			80	ps
			300 MHz				70	
			356 MHz				60	
			400 MHz				50	
t_r, t_f	Output rise and fall times (measured at 20%−80% of output voltage)			See Figure 7	160		400	ps
Δt	Difference between rise and fall times on a single device (20%−80%) $\lvert t_f - t_r \rvert$			See Figure 7			100	ps

† All typical values are at V_{DD} = 3.3 V, T_A = 25°C.
‡ Assured by design

state transition latency specifications

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{(powerup)}$	Delay time, PWRDNB↑ to CLK/CLKB output settled (excluding $t_{(DISTLOCK)}$)	Powerdown	Normal	See Figure 8			3	ms
	Delay time, PWRDNB↑ to internal PLL and clock are on and settled						3	
$t_{(VDDpowerup)}$	Delay time, power up to CLK/CLKB output settled	V_{DD}	Normal	See Figure 8			3	ms
	Delay time, power up to internal PLL and clock are on and settled						3	
$t_{(MULT)}$	MULT0 and MULT1 change to CLK/CLKB output resettled (excluding $t_{(DISTLOCK)}$)	Normal	Normal	See Figure 9			1	ms
$t_{(CLKON)}$	STOPB↑ to CLK/CLKB glitch-free clock edges	CLK Stop	Normal	See Figure 10			10	ns
$t_{(CLKSETL)}$	STOPB↑ to CLK/CLKB output settled to within 50 ps of the phase before STOPB was disabled	CLK Stop	Normal	See Figure 10			20	cycles
$t_{(CLKOFF)}$	STOPB↓ to CLK/CLKB output disabled	Normal	CLK Stop	See Figure 10			5	ns

† All typical values are at V_{DD} = 3.3 V, T_A = 25°C.

state transition latency specifications (continued)

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{(powerdown)}$	Delay time, PWRDNB↓ to the device in the power-down mode	Normal	Powerdown	See Figure 8			1	ms
$t_{(STOP)}$	Maximum time in CLKSTOP (STOPB = 0) before reentering normal mode (STOPB = 1)	STOPB	Normal	See Figure 10			100	µs
$t_{(ON)}$	Minimum time in normal mode (STOPB = 1) before reentering CLKSTOP (STOPB = 0)	Normal	CLK stop	See Figure 10	100			ms
$t_{(DISTLOCK)}$	Time from when CLK/CLKB output is settled to when the phase error between SYNCLKN and PCLKM falls within $t_{(phase)}$	Unlocked	Locked				5	ms

† All typical values are at V_{DD} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

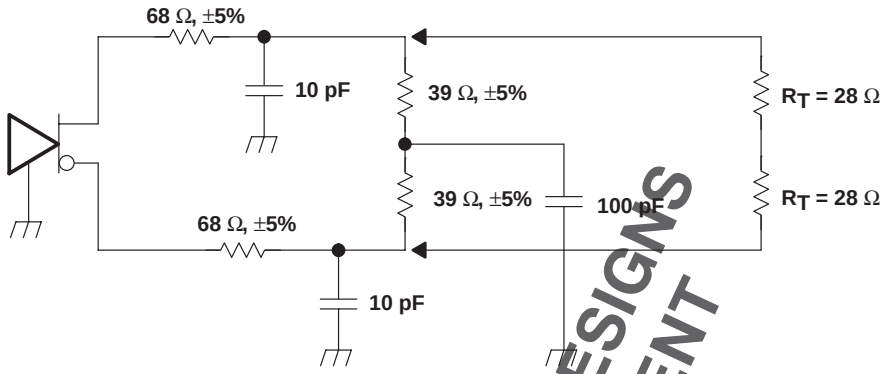
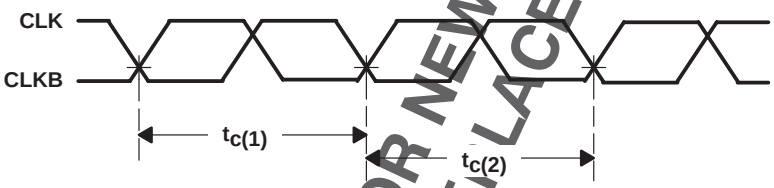
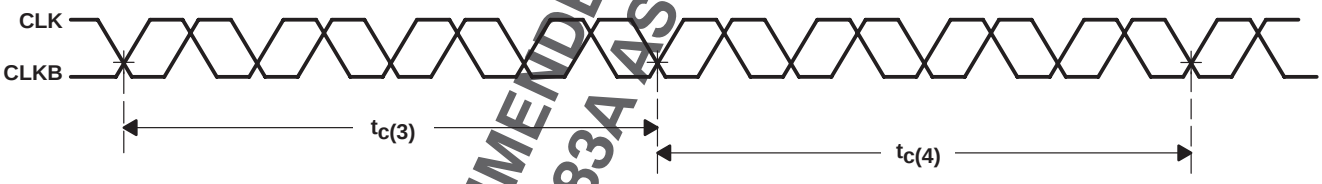


Figure 1. Test Load and Voltage Definitions ($V_{O(STOP)}$, $V_{O(X)}$, V_O, V_{OH}, V_{OL})



Cycle-to-cycle jitter = $| t_{c(1)} - t_{c(2)} |$ over 10000 consecutive cycles

Figure 2. Cycle-to-Cycle Jitter



Cycle-to-cycle jitter = $| t_{c(3)} - t_{c(4)} |$ over 10000 consecutive cycles

Figure 3. Short Term Cycle-to-Cycle Jitter Over Four Cycles

PARAMETER MEASUREMENT INFORMATION

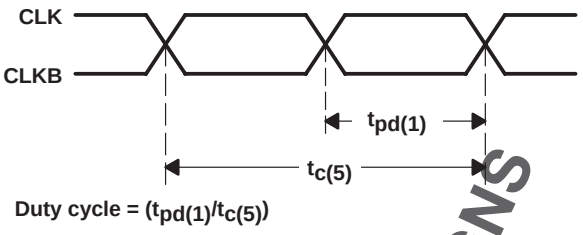


Figure 4. Output Duty Cycle

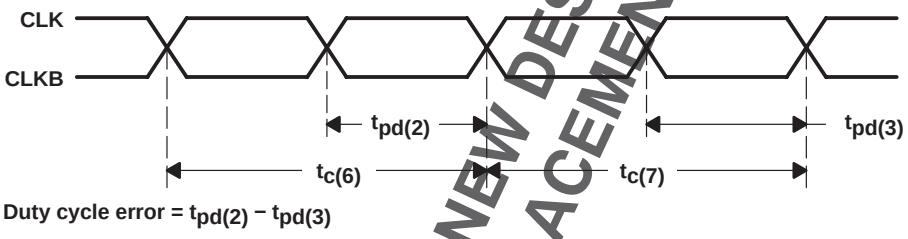


Figure 5. Duty Cycle Error (Cycle-to-Cycle)

Figure 6. Crossing-Point Voltage

Figure 7. Voltage Waveforms

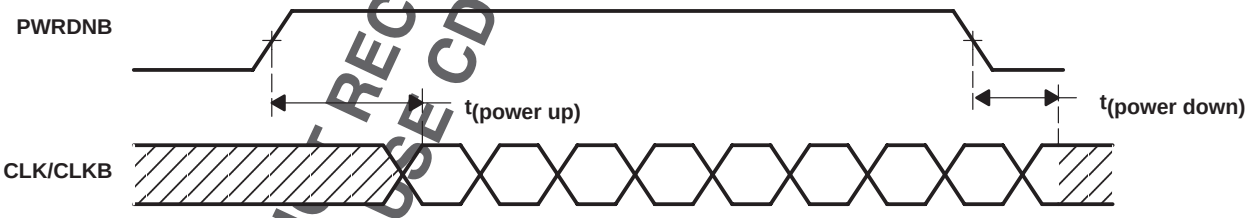


Figure 8. PWRDNB Transition Timings

PARAMETER MEASUREMENT INFORMATION

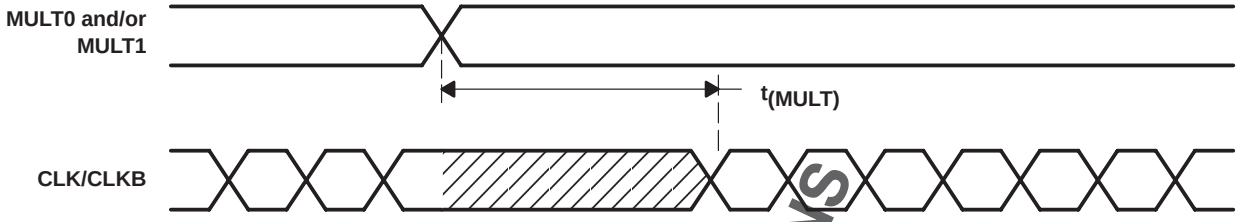
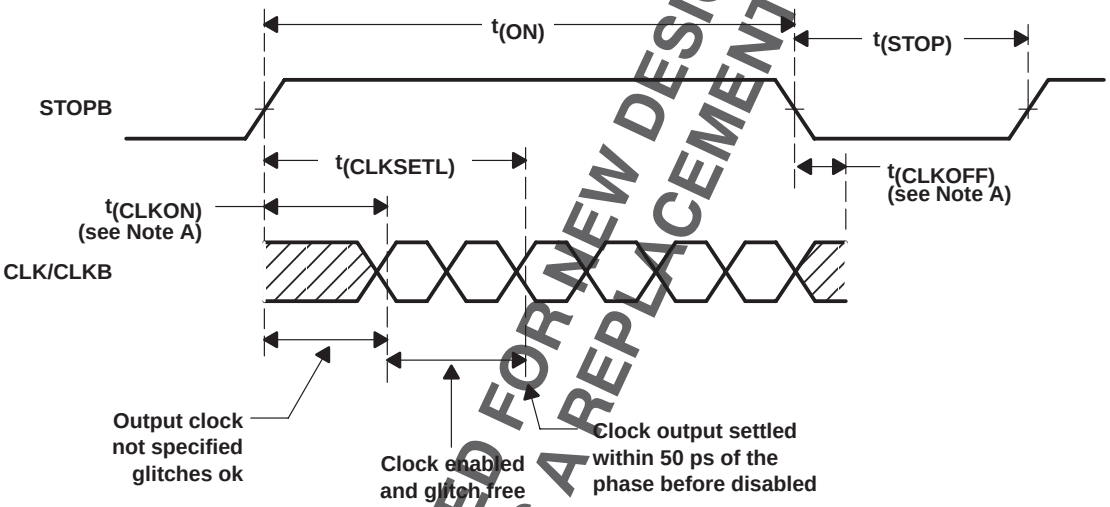


Figure 9. MULT Transition Timings



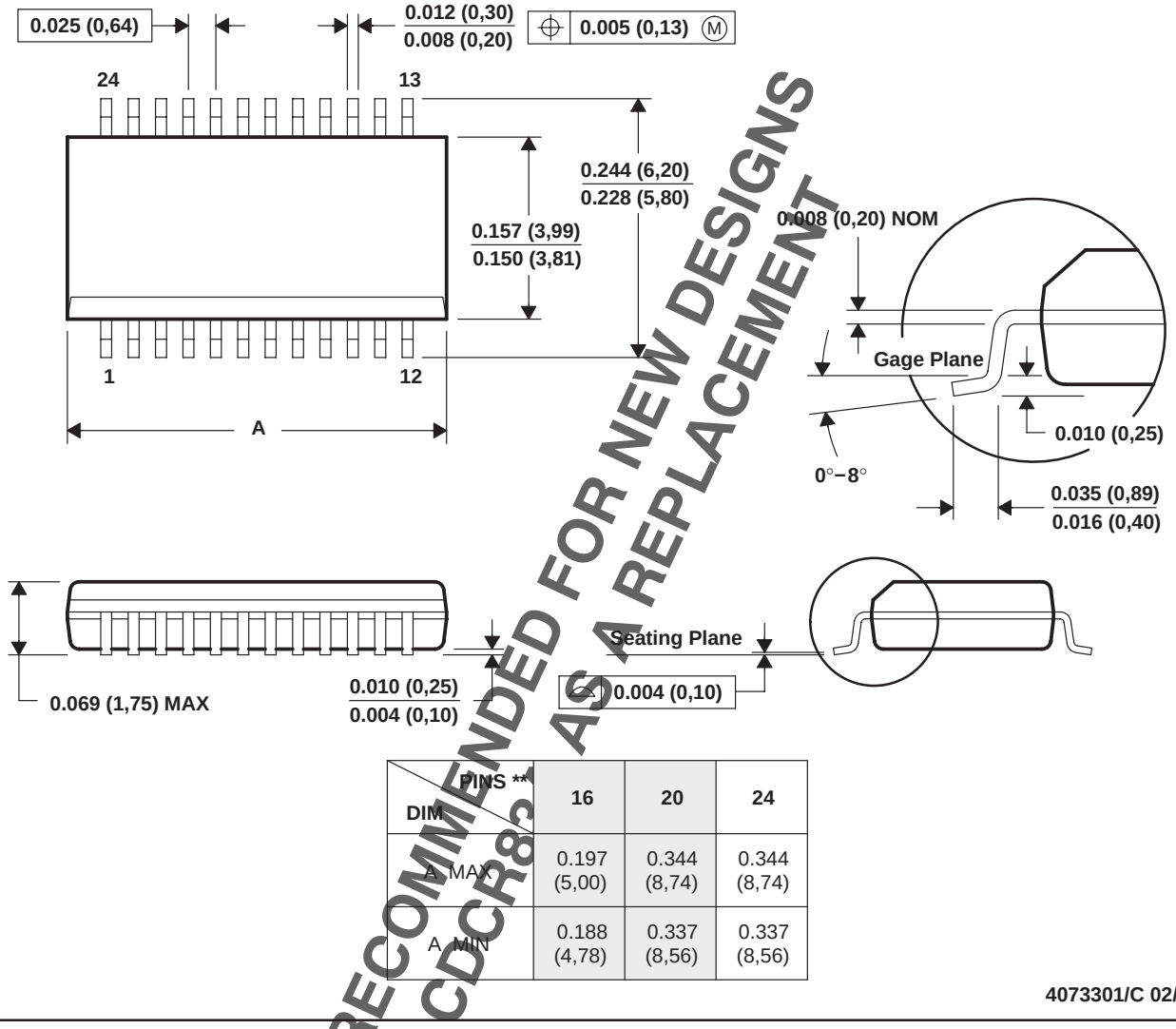
NOTE A: $V_{ref} = V_O \pm 200$ mV

Figure 10. STOPB Transition Timings

MECHANICAL DATA

DBQ (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

24-PIN SHOWN



DIM \ PINS **	16	20	24
A MAX	0.197 (5,00)	0.344 (8,74)	0.344 (8,74)
A MIN	0.188 (4,78)	0.337 (8,56)	0.337 (8,56)

4073301/C 02/97

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-137

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CDCR83DBQ	NRND	SSOP/ QSOP	DBQ	24	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CDCR83DBQG4	NRND	SSOP/ QSOP	DBQ	24	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CDCR83DBQR	NRND	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CDCR83DBQRG4	NRND	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

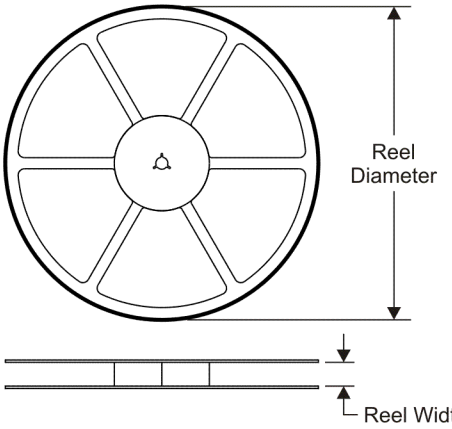
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

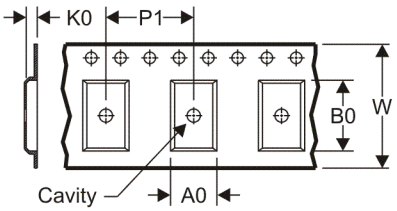
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

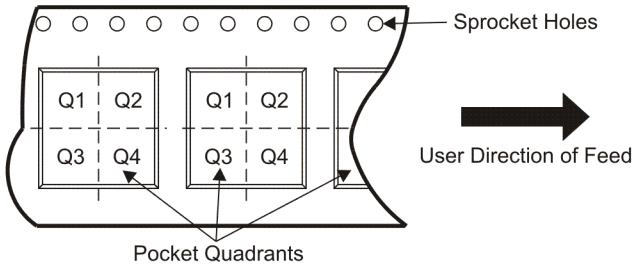


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

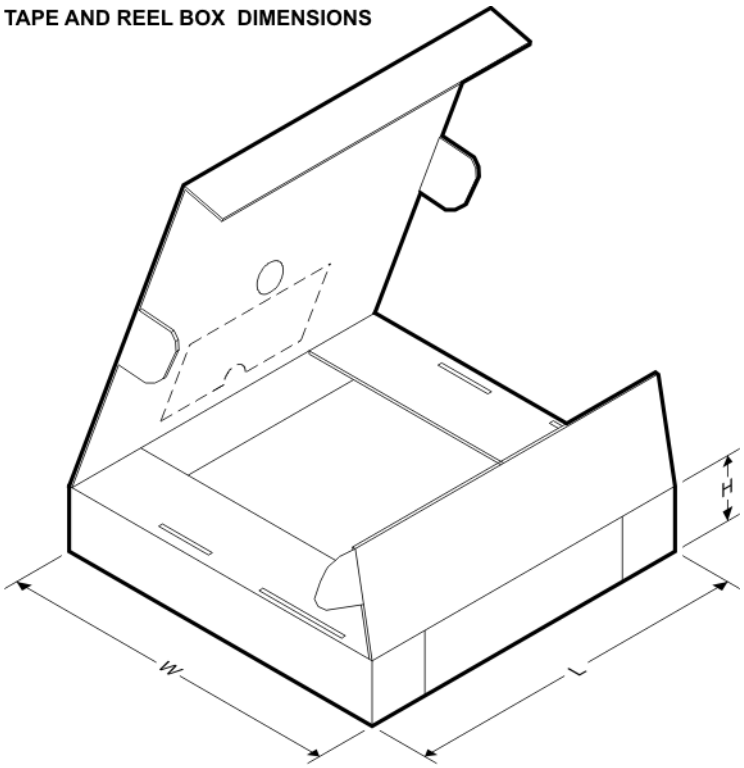
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCR83DBQR	SSOP/ QSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCR83DBQR	SSOP/QSOP	DBQ	24	2500	346.0	346.0	33.0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Clocks and Timers	www.ti.com/clocks	Digital Control	www.ti.com/digitalcontrol
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265